AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method for use in a receiver comprising:

separating real and imaginary components of a received signal;

equalizing the imaginary component of the received signal;

using the real component of the received signal in controlling a timing in the receiver; and

using the imaginary component but not the real component of the received signal in an equalization adaptation procedure.

2. (Previously Presented) The method in claim 1, wherein the received signal is a known signal.

3. (Previously Presented) The method in claim 1, wherein the received signal is a pilot tone.

4. (Previously Presented) The method in claim 1, wherein controlling the timing includes adjusting a sampling rate of the receiver for sampling the received signal.

5. (Previously Presented) The method in claim 1, wherein controlling the timing includes synchronizing the timing signal in the receiver with a timing signal in a transmitter that transmitted the signal received by the receiver.

6. (Previously Presented) The method in claim 1, wherein the equalization adaptation procedure includes updating an equalizer coefficient value.

7. (Previously Presented) The method in claim 6, wherein the imaginary component is equalized using the equalizer coefficient value.

8. (Previously Presented) The method in claim 7, further comprising:

determining an error between an actual value of the received signal and the equalized imaginary component signal, and

using the error to update the equalizer coefficient value.

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9. (Previously Presented) The method in claim 6, wherein only the imaginary component of the received signal is equalized.

10. (Previously Presented) The method in claim 6, wherein both the real and imaginary components of the received signal are equalized.

11. (Previously Presented) The method in claim 10, further comprising:

determining an equalizer coefficient value corresponding to the known signal, and

updating both the real and imaginary components of the known signal with the equalizer coefficient value.

12. (Previously Presented) The method in claim 1, wherein the real component but not the imaginary component of the received signal is used in controlling the timing of the receiver.

13. (Previously Presented) The method in claim 1, wherein the receiver is a discrete multitone receiver, and the equalization procedure is implemented in the frequency domain.

14. (Previously Presented) The method in claim 1, further comprising:

combining the real component and the imaginary component after equalization to generate a complex output signal.

15. (Previously Presented) The method in claim 1, wherein the real component is filtered and applied to a voltage controlled oscillator coupled to an analog to digital converter in the receiver.

16. (Previously Presented) A receiver, comprising:

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an analog-to-digital converter for sampling a received signal including a known signal;

an equalizer for equalizing the sampled signal except for a real component of the known signal; and

a timing control unit for controlling the analog-to-digital converter,

wherein the real component of the known signal is used to control the timing unit.

17. (Previously Presented) The receiver in claim 16, wherein the receiver is a discrete multitone receiver employing plural subcarriers to convey information, and the equalizer is a frequency domain equalizer, the receiver further comprising:

a serial to parallel converter converting an output of the analog to digital converter to parallel time domain samples corresponding the plural subcarriers, and

a fast Fourier transform processor transforming the parallel time domain samples into parallel frequency domain samples which are provided to the frequency domain equalizer.

18. (Previously Presented) The receiver in claim 16, wherein the timing control unit is a voltage-controlled oscillator, and wherein the real component of the known signal is filtered.

19. (Previously Presented) The receiver in claim 16, wherein the equalizer sets the real component of the known signal to zero and equalizes an imaginary component of the known signal and adds the real component of the known signal to the equalized, imaginary component of the known signal.

20. (Previously Presented) The receiver in claim 19, wherein the equalizer adapts an equalizer coefficient corresponding to the known signal using the equalized, imaginary component of the known signal but not the real component of the known signal.

21. (Previously Presented) A receiver, comprising:

an analog-to-digital converter for sampling a received signal including a known signal;

an equalizer for equalizing the sampled signal, where the same equalizer coefficient is used to update both real and imaginary components of the known signal; and

a timing control unit for controlling the analog to digital converter,

wherein the equalized, real component of the known signal is used to control the timing unit, and

wherein the same equalizer coefficient is a real-valued equalizer coefficient which is updated using the imaginary component but not the real component.

22. (Cancelled)

23. (Previously Presented) The receiver in claim 21, wherein the receiver is a discrete multitone receiver employing plural subcarriers to convey information, and the equalizer is a frequency domain equalizer, the receiver further comprising:

a serial-to-parallel converter converting an output of the analog to digital converter to parallel time domain samples corresponding the plural subcarriers, and

a fast Fourier transform processor transforming the parallel time domain samples into parallel frequency domain samples which are provided to the frequency domain equalizer.

24. (Previously Presented) The receiver in claim 21, wherein the timing control unit is a voltage-controlled oscillator, and wherein the real component of the known signal is filtered.

25. (Currently Amended) A receiver, comprising:

an analog-to-digital converter for sampling a received signal including a known signal;

an equalizer for equalizing the sampled signal including:

a first mechanism to process a real component of the known signal, and

a second mechanism to process an imaginary component of the known signal; and

a timing control unit for controlling the analog to digital converter,

wherein one of the real and imaginary components of the known signal processed by the first and second mechanisms, respectively, is used to control the timing unit, and

wherein the first and second mechanisms permit simultaneous equalization of the known signal by the equalizer and recovery of a timing signal from the known signal at the timing control unit.

26. (Cancelled)

27. (Currently Amended) The receiver in claim ~~26~~ 25, wherein the equalizer updates an equalizer coefficient corresponding to the known signal.

28. (Currently Amend) The receiver in claim ~~26~~ 25, wherein the real component of the known signal is not equalized and the imaginary part of the known signal is equalized.

29. (Currently Amended) The receiver in claim ~~26~~ 25, wherein the real component of the known signal and the imaginary component of the known signal are both equalized using the same equalizer coefficient.

30. (Currently Amended) The receiver in claim ~~26~~ 25, wherein the real component of the known signal is used to control the timing unit.

31. (Currently Amended) The receiver in claim ~~26~~ 25, wherein the first and second mechanisms are decoupled.

32. (Currently Amended) The receiver in claim ~~26~~ 25, wherein the second mechanism sets the real component of the known signal to zero so that only the

imaginary part of the known signal is equalized, and wherein the first mechanism provides the unequalized real component of the known signal to control the timing unit.

33. (Currently Amended) The receiver in claim ~~26~~ 25, wherein the first mechanism equalizes the real component of the known signal with a real-valued equalizer coefficient which is then used to control the timing unit, and wherein the second mechanism equalizes the imaginary component with the real-valued equalizer coefficient, the equalized imaginary component being used by the second mechanism to determine an equalizer error to modify the real equalizer coefficient.

34. (Previously Presented) The receiver in claim 25, wherein the known signal is a pilot tone.

35. (Previously Presented) The receiver in claim 25, wherein the timing unit timing includes synchronizing the timing signal in the receiver with a timing signal in a transmitter that transmitted the signal received by the receiver.

36. (Previously Presented) The receiver in claim 25, wherein the receiver is a discrete multitone receiver, and the equalizer is a frequency domain equalizer.